PVP 17

Code: **17ECMC2T5C**

I M.Tech - II Semester – Regular Examinations – AUGUST 2018

DSP PROCESSORS
(MICROWAVE & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 60

Answer the following questions.

1. a) Explain about fixed point and floating point number representations for representing signals and coefficients. 8 M

   b) Write short notes on DSP computational errors. 7 M

OR

2. a) Consider a dsp device 16X16 multiplier interfaced to 16-bit A/D converter and 16-bit D/A converter. Calculate the SNR of the computations performed by the device. Assume. $\sigma_x^2 = \frac{1}{4}$ 8 M

   b) Briefly discuss about A/D conversion errors. 7 M

3. a) Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP? 8 M

b) Explain the architecture of MAC unit and discuss about working of saturation logic. 7 M

OR

4. Discuss in brief about the data addressing capabilities of programmable DSP devices with examples. 15 M

5. a) What is the function of Address Generation unit in TMS320C54XX Processors? 7 M

b) Describe the pipelining operation of TMS320C54XX processors. 8 M

OR

6. a) Identify the addressing modes of the operands in each of the following instructions & their operations. 8 M

i) ADD B ii) ADD #1234h

iii) ADD 5678h iv) ADD +*addreg

b) Explain the Interrupts of TMS320C54XX Processors. 7 M

7. a) With an example explain Q-notation. Explain how multiplication of numbers is represented using Q-notation? 7 M

b) Explain how images are processed using DSP processors? 8 M

OR

8. a) Mention the procedure to implement 8-point FFT algorithm on TMS320C54XX processor. 7 M

b) Briefly discuss about how PID controller can be implemented on TMS320C54XX processor? 8 M